



REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

Claims 1, 2, 4-8 and 10-26 are pending in this application. Claims 6-8, 10-15 and 19-26 are withdrawn from consideration. Claims 1 and 16 are amended by way of the present amendment. Claims 1-2 are rejected under 35 U.S.C. § 102(b) over Roman et al. (U.S. 4,053,924) and claims 1-2, 4-5 and 16-18 are rejected under 35 U.S.C. § 103(a) over Kuwahara (U.S. 5,444,271) in view of Roman et al.

The Applicants have submitted an Information Disclosure Statement with English abstracts for JP 64-47066, JP 10-004187 and EP0621640. Also submitted is U.S. 5,166,770, which appears to correspond to JP 64-47066, and U.S. 5,668,385, which appears to correspond to EP 0621640. EP0621640 was apparently not considered since a line was drawn through the reference in the 1449 form attached to the current Office Action. Consideration of the submitted references is respectfully requested.

Claim 1 is amended to recite an electrode section having a second-conductivity-type impurity layer formed in one surface of the semiconductor substrate and having a thickness of more than 0.2  $\mu\text{m}$  and not more than 1.0  $\mu\text{m}$  from the one surface of the semiconductor substrate. This is shown, for example, in Fig. 2 of the present application and is supported by, for example, lines 18-27 of page 12 where the region 4 is interposed between the layer 2 and the electrode 3, providing that region 2 is larger than region 4. Also, the peak of the impurity concentration is at a portion shallower than 0.2  $\mu\text{m}$  from the surface of a substrate. With such a device, both a decrease in the contact resistance and an increase in the turn-off speed can be achieved. Accordingly, the prior art cannot produce the advantages of the present invention.

It is respectfully submitted that the cited prior art does not disclose or suggest the electrode section of claim 1. Roman et al., as pointed out in the Office Action, discloses a

diode 25 having a p+ region 32 having a thickness of 0.03-0.08  $\mu\text{m}$  and a p region 34 having a thickness from 0.35 to 0.1  $\mu\text{m}$ .. The thickness of region 34 is not more than 0.2  $\mu\text{m}$  as recited in claim 1. As Roman et al. clearly does not disclose the electrode section of claim 1, claim 1 is patentable over Roman et al. Withdrawal of the rejection is respectfully requested.

Kuwahara merely shows examples of an IGBT structure and the impurity concentration of an impurity layer. There is no disclosure or suggest of the impurity and contact layers having the thicknesses recited in claim 1, as recognized in the Office Action. Accordingly, it is clear that claim 1 is patentable over a combination of Kuwahara and Roman et al. and withdrawal of the rejection over this combination is also respectfully requested.

Claim 16 recites a device having a second-conductivity-type impurity region formed in another surface of the semiconductor substrate and having a thickness of more than 0.2  $\mu\text{m}$  and not more than 1.0  $\mu\text{m}$  from the another surface of the semiconductor substrate. This is not disclosed in Roman et al. where the regions 32 and 34 have thicknesses in the ranges of 0.03-0.08  $\mu\text{m}$  and 0.35 to 0.1  $\mu\text{m}$ , respectively. Kuwahara also does not disclose or suggest the thicknesses for the impurity and contact layers recited in claim 16, as recognized in the Office Action. Accordingly, it is clear that claim 16 is patentable over a combination of Kuwahara and Roman et al. and withdrawal of the rejection over this combination is respectfully requested.

It is therefore respectfully submitted that the present application is in condition for allowance and a favorable decision to that effect is respectfully requested.

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